

SOLIOS EV-CL CAMERA LINK FRAME GRABBER

SOL2MEVCLB

MTX FG PCIe SOL CL X4 256MB

- Frame grabber with available support for 10-taps
- Captures from frame and line scan cameras
- Programmable FPGA (optional)
- PCI Express x4 interface



PRODUCT DESCRIPTION

Matrox Solios eV-CL ushers in a new level of value for Camera Link® frame grabbers. It provides connectivity to the most high-performance, multi-megapixel area and line scan Camera Link® cameras on the market augmented with onboard Bayer interpolation (eV-CLB/CLBL), color space conversions and look-up tables. The Matrox Solios eV-CL provides all these capabilities at the most attractive price point yet.

TECHNICAL SPECIFICATIONS

Connectivity (ev-CLB/CLF)	Connectivity (ev-CLBL/CLFL)
<ul style="list-style-type: none"> • two(2) mini Camera Link® (HDR) connectors • one (1) DBHD-15 male connector <ul style="list-style-type: none"> • three (3) TTL configurable auxiliary I/Os • two (2) LVDS auxiliary inputs • one (1) LVDS auxiliary output • two (2) opto-isolated auxiliary inputs • optional add on DBHD-15 male connector <ul style="list-style-type: none"> • three (3) TTL configurable auxiliary I/Os • two (2) LVDS auxiliary inputs • one (1) LVDS auxiliary output • two (2) opto-isolated auxiliary inputs • optional add on DB-91 female connector <ul style="list-style-type: none"> • one (1) TTL configurable auxiliary I/O • one (1) LVDS auxiliary input • two (2) opto-isolated auxiliary inputs 	<ul style="list-style-type: none"> • two(2) Camera Link® (MDR) connectors • one DB-44 and DB-9 connector <ul style="list-style-type: none"> • six (6) TTL configurable auxiliary I/Os • four (4) LVDS configurable auxiliary inputs • four (4) LVDS configurable auxiliary outputs • separate LVDS pixel clock, hsync and vsync outputs • four (4) opto-isolated configurable auxiliary inputs

BLOCK DIAGRAM

Matrox Solios eV-CLB

